Chapter 36. Chipsets and hubs

Since 1997, there has been more and more focus on refinement of the chipset, and not least the north bridge, which looks after data transfer to and from RAM. The south bridge has also been constantly developed, but the focus has been on adding new facilities.

For the north bridge, the development has focused on getting more bandwidth between the RAM and CPU. Let's look at a few examples of this.

Bridge or Hub

In a Pentium II motherboard, the I/O bus is directly linked to the system clock. The I/O bus (that is, in practise, the PCI bus) runs at 33 MHz, and that is typically a third or a quarter of the system clock speed (see Fig. 121).

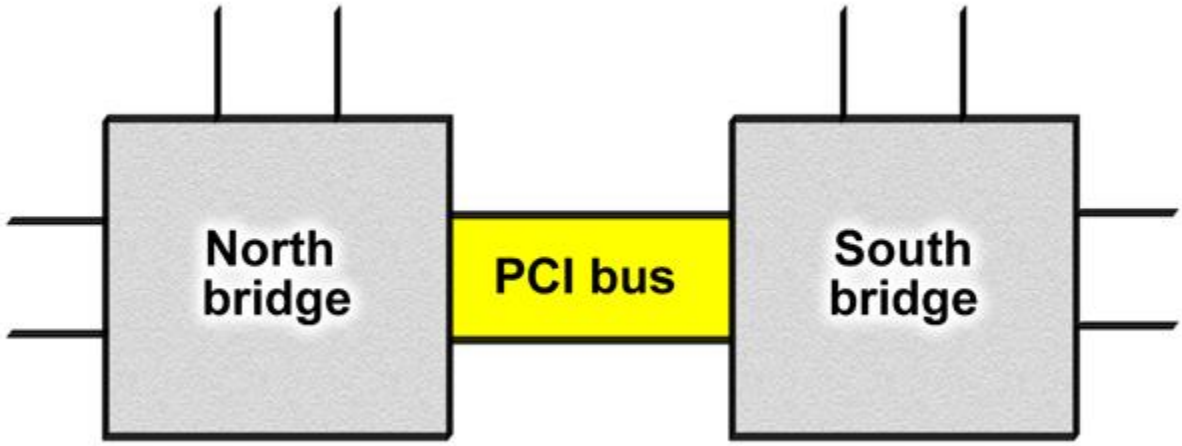

Figure 145. In this architecture (from the Pentium II chipset), the PCI bus connects to the chipset's two bridges.

In 1998-99, new developments took place at both AMD and Intel. A new architecture was introduced based on a Memory Controller Hub (*MCH*) instead of the traditional north bridge and an I/O Controller Hub (*ICH*) instead of the south bridge. I am using Intel's names here; the two chips have other names at AMD and VIA, but the principle is the same. The first Intel chipset with this architecture was called *i810*.

The MCH is a controller located between the CPU, RAM and AGP. It regulates the flow of data to and from RAM. This new architecture has two important consequences:

- The connection between the two *hubs* is managed by a special bus (*link channel*), which can have a very high bandwidth.
- The PCI bus comes off the ICH, and doesn't have to share its bandwidth with other devices.

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The new architecture is used for both Pentium 4 and Athlon processors, and in chipsets from Intel, VIA, and others. In reality, it doesn't make a great deal of difference whether the chipset consists of hubs or bridges, so in the rest of the guide I will use both names indiscriminately.

Figure 146. The MCH is the central part of the i875P chip set.

The i875P chipset

In 2003, Intel launched a chipset which work with the Pentium 4 and dual channel DDR RAM, each running at 200 MHz. This chip set became very popular, since it had a very good performance.

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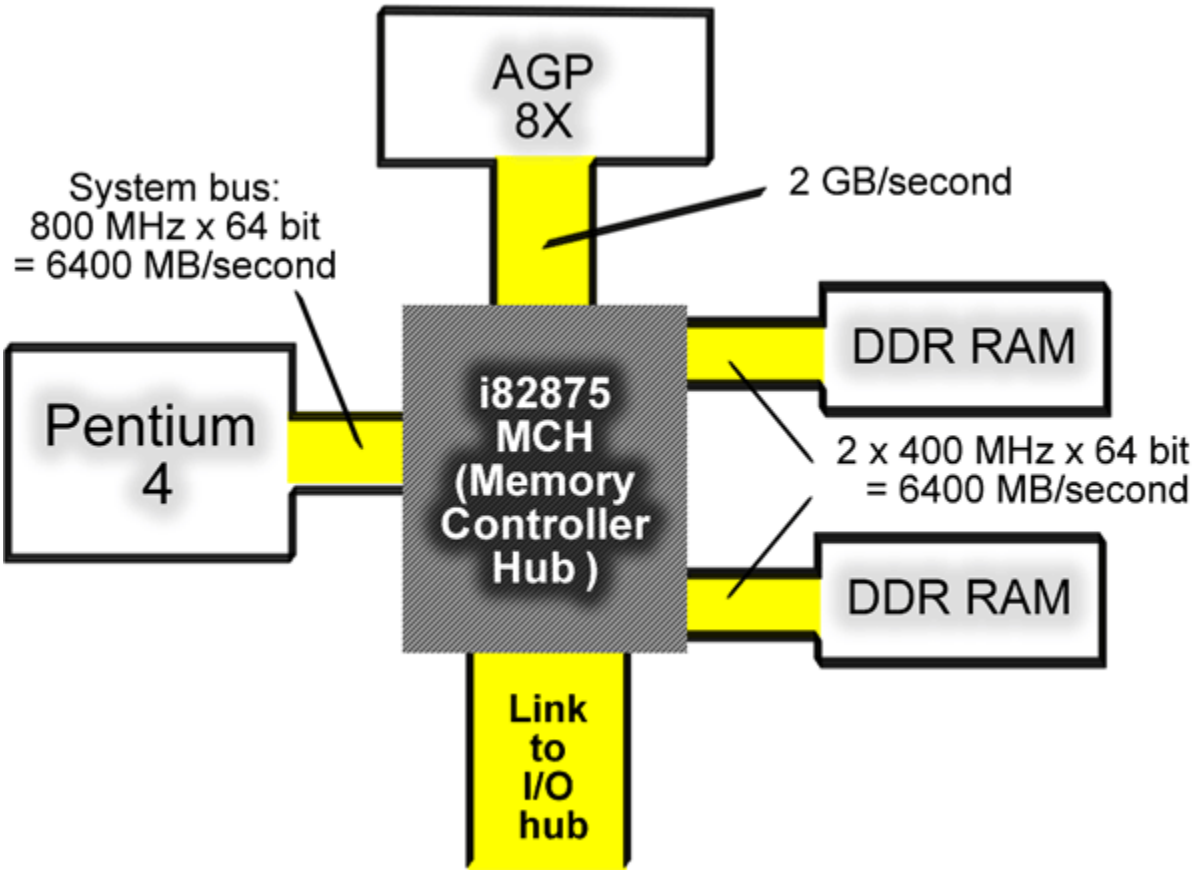

Figure 147. The architecture surrounding the Intel® 82875P Memory Controller Hub (MCH).

Another new feature in this chip set is that a Gigabit Ethernet controller can have direct access to the MCH (the north bridge). Traditionally the LAN controller is connected to the PCI bus. But since a gigabit network controller may consume a great band width, it is better to plug it directly into north bridge. This new design is called Communication Streaming Architecture (CSA).

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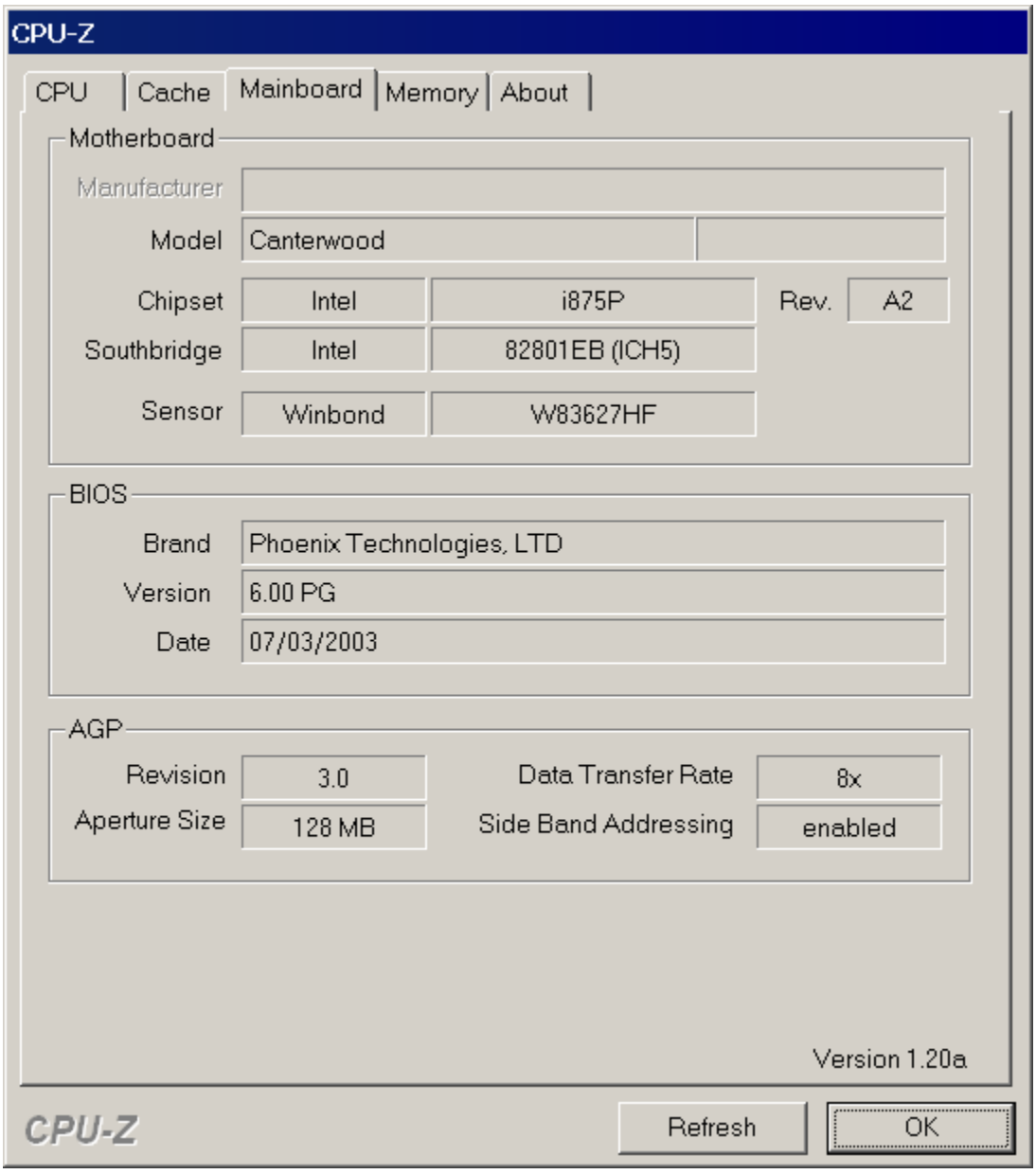

Figure 148. Report from the freeware program CPU-Z.

The i925 chipset

In late 2004 Intel introduced a new 900-series of chipsets. They were intended for the new generation of Pentium 4 and Celeron processors based on the LGA 775-socket (as in Figur 112. The chip sets comes with support for the PCI Express bus, which is replacing the AGP bus and with support of DDR2 RAM:

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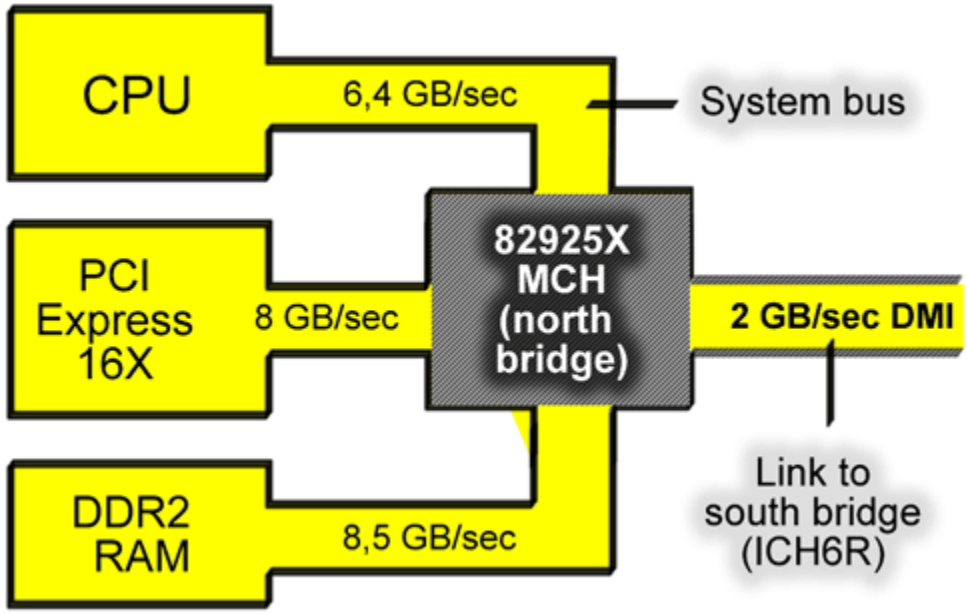

Figure 149. The new chipset architecture, where the north bridge has become a hub. Here Intel chip set i925.

By making use of dual channel DDR2 RAM, a bandwidth of up to 8.5 GB/sec is achieved.

Big bandwidth for RAM

One might be tempted to think that the bandwidth to the RAM ought to be identical with that of the system bus. But that is not the case. It would actually be good if it was higher. That's because the RAM doesn't only deliver data to the CPU. Data also goes directly to the graphics port and to and from the I/O devices – bypassing the CPU. RAM therefore needs even greater bandwidth. In future architectures we will see north bridges for both Pentium 4 and Athlon XP processors which employ more powerful types of RAM, such as 533 MHz DDR2.

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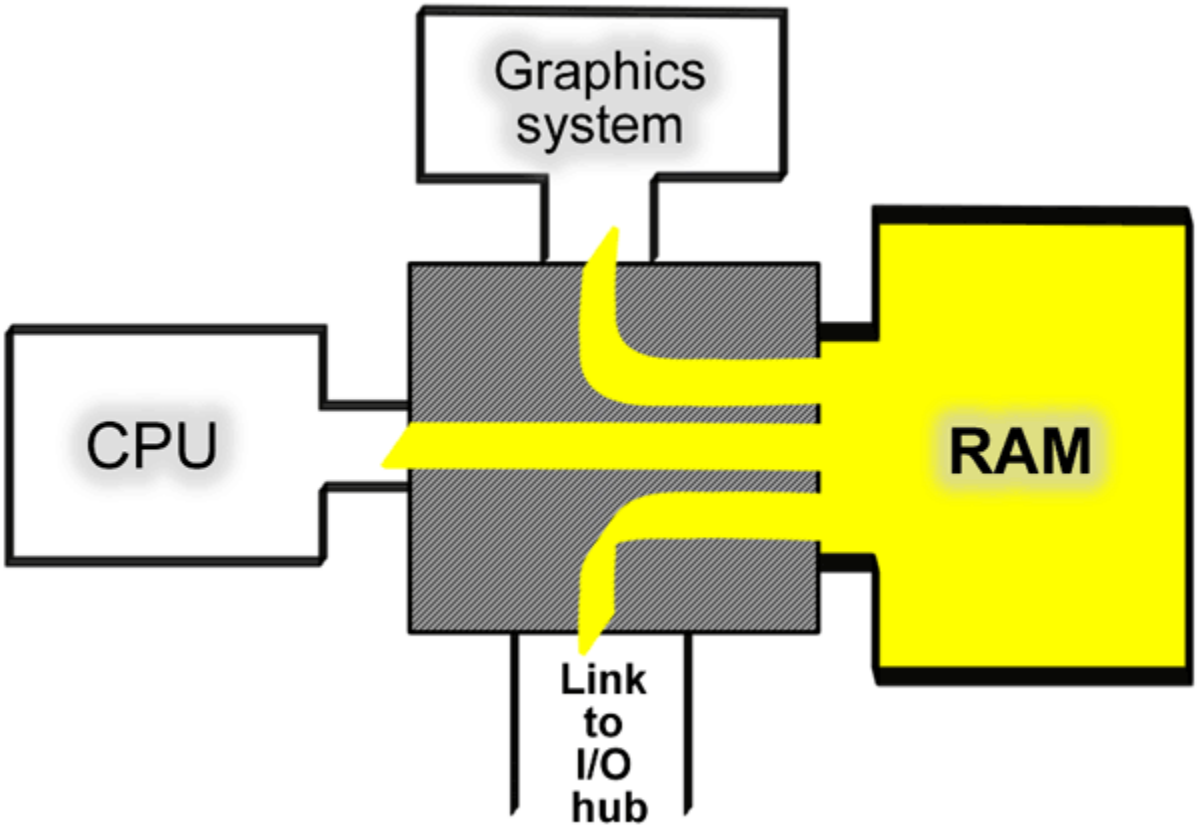

Figure 150. In reality, the RAM needs greater bandwidth than the CPU.